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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,880	HAYCOCK ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6,7 and 14-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,7 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the Applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the Applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 3, 6, 7, 14, 15, and 16 rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Number 6,601,196 to Dabral et al. ("Dabral")

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

3. In reference to Claim 1, Dabral discloses an apparatus comprising a buffer having a trigger, integrated on a component connected with a simultaneous bi-

directional (SBD) memory bus having ternary logic levels (See Figure 2 Number 250, Column 1 Lines 12-14, and Column 3 Lines 15-18), to facilitate observing and echoing of one or more of a plurality of signals transmitted on said memory bus (See Column 3 Lines 7-10), wherein the trigger operates to instruct the buffer using a control signal based indication (See Column 1 Lines 14-17 and Column 3 Lines 7-10), and a time-based indication (See Column 1 Lines 14-17). The trigger of Dabral will inherently instruct the buffer using an address-signal based indication, as the device of Dabral is used in a system for transferring data between devices that include processors, storage devices, and I/O devices (See Column 1 Lines 12-14), and as such would inherently include address signals.

4. In reference to Claim 2, Dabral discloses the limitations as applied to Claim 1 above. Dabral further discloses an observability port coupled with said buffer to receive said echoed signals (See Figure 2 Numbers 258 and 259 and Column 3 Lines 7-10), an observability bus connected with said observability port (See Figure 2 Numbers 291 and 292), and a diagnostic device being at least one of a logic analyzer and a bus analyzer connected with said observability bus and performing at least one of detecting said echoed signals, accessing said echoed signals and reading said echoed signals (See Figure 2 Number 290 and Column 3 Lines 4-14).

5. In reference to Claim 3, Dabral discloses the limitations as applied to Claim 2 above. Dabral further discloses that said observability port is a logic observability port (See Column 3 Lines 10-14).

6. In reference to Claim 6, Dabral discloses a method comprising transmitting a plurality of signals on a simultaneous bi-directional (SBD) memory bus having ternary logic level; a buffer having a trigger, integrated on a component connected with the bus (See Figure 2 Number 250, Column 1 Lines 12-14, and Column 3 Lines 15-18), to facilitate observing and echoing of one or more of a plurality of signals transmitted on the bus (See Column 3 Lines 7-10), wherein the trigger operates to instruct the buffer using a control signal based indication (See Column 1 Lines 14-17 and Column 3 Lines 7-10), and a time-based indication (See Column 1 Lines 14-17). The trigger of Dabral will inherently instruct the buffer using an address-signal based indication, as the device of Dabral is used in a system for transferring data between devices that include processors, storage devices, and I/O devices (See Column 1 Lines 12-14), and as such would inherently include address signals.

7. In reference to Claim 7, Dabral discloses the limitations as applied to Claim 6 above. Dabral further discloses receiving said echoed signals (See Figure 2 Numbers 258 and 259 and Column 3 Lines 7-10); and performing at least one of detecting said echoed signals, accessing said echoed signals and reading said echoed signals (See Figure 2 Number 290 and Column 3 Lines 4-14).

8. In reference to Claim 14, Dabral discloses a memory (See Column 1 Lines 12-14); an input/output (I/O) port (See Column 1 Lines 12-14); a microprocessor (See Column 1 Lines 12-14); and a buffer, having a trigger, integrated on a component coupled with a simultaneous bi-directional (SBD) memory bus having ternary logic levels (See Figure 2 Number 250, Column 1 Lines 12-14, and Column 3 Lines 15-18), to facilitate observing and echoing a plurality of signals transmitted on said bus (See Column 3 Lines 7-10), wherein the trigger operates to instruct the buffer using a control signal based indication (See Column 1 Lines 14-17 and Column 3 Lines 7-10), and a time-based indication (See Column 1 Lines 14-17). The trigger of Dabral will inherently instruct the buffer using an address-signal based indication, as the device of Dabral is used in a system for transferring data between devices that include processors, storage devices, and I/O devices (See Column 1 Lines 12-14), and as such would inherently include address signals.

9. In reference to Claim 15, Dabral discloses the limitations as applied to Claim 14 above. Dabral further discloses an observability port coupled with said buffer to receive said echoed signals (See Figure 2 Numbers 258 and 259 and Column 3 Lines 7-10), an observability bus connected with said observability port (See Figure 2 Numbers 291 and 292), and a diagnostic device being at least one of a logic analyzer and a bus analyzer connected with said observability bus and performing at least one

of detecting said echoed signals, accessing said echoed signals and reading said echoed signals (See Figure 2 Number 290 and Column 3 Lines 4-14).

10. In reference to Claim 16, Dabral discloses the limitations as applied to Claim 15 above. Dabral further discloses that said observability port is a logic observability port (See Column 3 Lines 10-14).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1, 2, 6, 7, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,933,594 to La Joie et al. ("La Joie"), US Patent Number 5,666,302 to Tanaka et al. ("Tanaka") and knowledge which is well known in the art.

13. In reference to Claim 1, La Joie teaches a buffer having a trigger (See Figure 1, Column 13 Lines 58-67, and Column 14 Lines 1-34); capturing a plurality of signals by a monitoring system, which is equivalent to observing and echoing signals (See

Column 2 Lines 34-41), from a bus, and wherein the trigger operates to instruct the buffer using a control signal-based indication (See Column 13 Lines 36-42). La Joie does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. Tanaka teaches the use of a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55). The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the simultaneous bi-directional bus of Tanaka with the bus monitoring system of La Joie, resulting in the invention of Claim 1, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie).

14. In reference to Claim 2, La Joie, Tanaka, and knowledge commonly known in the art teach the limitations as applied to Claim 1 above. La Joie further teaches an observability bus, connected between a port on the analyzer buffer, which is equivalent to the observability port (See Figure 1 and Column 14 Lines 4-15) and the analyzer logic control, which is equivalent to the logic analyzer and bus analyzer (See Figure 1, Column 13 Lines 60-67, and Column 14 Lines 1-4) to receive the signals (See Column 13 Lines 34-36); capturing the external signal, which is equivalent to detecting the

signal (See Column 13 Lines 36-38); defining a data capture window, which is equivalent to accessing the signal (See Column 14 Lines 13-15); and storing the data in the analyzer buffer, which is equivalent to reading the signal (See Column 14 Lines 4-5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the simultaneous bi-directional bus of Tanaka with the bus monitoring system of La Joie, resulting in the invention of Claim 2, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie).

15. In reference to Claim 6, La Joie teaches a buffer having a trigger (See Figure 1, Column 13 Lines 58-67, and Column 14 Lines 1-34); capturing a plurality of signals by a monitoring system, which is equivalent to observing and echoing signals (See Column 2 Lines 34-41) from the bus, and wherein the trigger operates to instruct the buffer using a control signal-based indication (See Column 13 Lines 36-42). La Joie does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. Tanaka teaches the use of a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55). The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the simultaneous bi-directional bus of Tanaka with the bus monitoring system of La Joie, resulting in the invention of Claim 6, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie).

16. In reference to Claim 7, La Joie, Tanaka, and knowledge commonly known in the art teach the limitations as applied to Claim 6 above. La Joie further teaches receiving the signals (See Column 13 Lines 34-36); capturing the signal, which is equivalent to detecting the signal (See Column 13 Lines 36-38); defining a data capture window, which is equivalent to accessing the signal (See Column 14 Lines 13-15); and storing the data in the analyzer buffer, which is equivalent to reading the signal (See Column 14 Lines 4-5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the simultaneous bi-directional bus of Tanaka with the bus monitoring system of La Joie, resulting in the invention of Claim 7, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie).

17. In reference to Claim 14, La Joie teaches a memory (See Figure 1 Number 22); an I/O port (See Figure 1 Number 28); a microprocessor (See Figure 1 Number 10); a processor bus connecting the memory, I/O port, and microprocessor (See Figure 1

Number 12); and a buffer having a trigger (See Figure 1 Number 20) that stores data captured from the bus, which is equivalent to observing and echoing signals (See Column 14 Lines 1-13) from the bus, and wherein the trigger operates to instruct the buffer using a control signal-based indication (See Column 13 Lines 36-42). La Joie does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. Tanaka teaches the use of a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55). The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the simultaneous bi-directional bus of Tanaka with the bus monitoring system of La Joie, resulting in the invention of Claim 14, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie).

18. In reference to Claim 15, La Joie, Tanaka, and knowledge commonly known in the art teach the limitations as applied to Claim 14 above. La Joie further teaches an observability bus, connected between a port on the analyzer buffer, which is equivalent to the observability port (See Figure 1 and Column 14 Lines 4-15) and the analyzer logic control, which is equivalent to the logic analyzer and bus analyzer (See Figure 1,

Column 13 Lines 60-67, and Column 14 Lines 1-4) to receive the signals (See Column 13 Lines 34-36); capturing the external signal, which is equivalent to detecting the signal (See Column 13 Lines 36-38); defining a data capture window, which is equivalent to accessing the signal (See Column 14 Lines 13-15); and storing the data in the analyzer buffer, which is equivalent to reading the signal (See Column 14 Lines 4-5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the simultaneous bi-directional bus of Tanaka with the bus monitoring system of La Joie, resulting in the invention of Claim 15, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie).

19. Claims 3 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beyers, La Joie, Tanaka, and knowledge commonly known in the art as applied to Claims 2 and 15 above, and further in view of US Patent Number 6,496,583 to Nakamura et al. ("Nakamura").

20. In reference to Claim 3, La Joie, Tanaka, and knowledge commonly known in the art teach the limitations as applied to Claim 2 above. La Joie, and Tanaka do not teach that the observability port is a logic observability port. Nakamura teaches a device that contains logic ports as an interface (See Figure 8 and Column 2 Lines 57-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of La Joie, and Tanaka with the device of Nakamura, resulting in the invention of Claim 3, in order to provide a means for converting the data at the port into a format compatible with the bus and devices connected to the port (See Column 3 Lines 23-27 of Nakamura).

21. In reference to Claim 16, La Joie, Tanaka, and knowledge commonly known in the art teach the limitations as applied to Claim 15 above. La Joie, and Tanaka do not teach that the observability port is a logic observability port. Nakamura teaches a device that contains logic ports as an interface (See Figure 8 and Column 2 Lines 57-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Beyers, La Joie, and Tanaka with the device of Nakamura, resulting in the invention of Claim 16, in order to provide a means for converting the data at the port into a format compatible with the bus and devices connected to the port (See Column 3 Lines 23-27 of Nakamura).

22. Claims 1, 6, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,488,688 to Gonzales et al. ("Gonzales"), Tanaka, and knowledge commonly known in the art.

23. In reference to Claim 1, Gonzales teaches a buffer having a trigger (See Column 2 Lines 23-26), integrated on a component connected with a bus (See Figure 1 and Column 2 Lines 23-26), to facilitate observing and echoing of one or more of a plurality of signals transmitted on said bus (See Column 2 Lines 23-26), wherein the trigger operates to instruct the buffer using a control signal-based indication (See Column 2 Lines 23-31). Gonzales does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. Tanaka teaches the use of a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55). The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Gonzales with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 1, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

24. In reference to Claim 6, Gonzales teaches a buffer having a trigger (See Column 2 Lines 23-26), integrated on a component connected with a bus (See Figure 1 and Column 2 Lines 23-26), to facilitate observing and echoing of one or more of a plurality of signals transmitted on the bus (See Column 2 Lines 23-26), wherein the

trigger operates to instruct the buffer using a control signal-based indication (See Column 2 Lines 23-31). Gonzales does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. Tanaka teaches the use of a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55). The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Gonzales with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 6, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

25. In reference to Claim 14, Gonzales inherently includes a memory and an I/O port. Gonzalez teaches a microprocessor (See Figure 1 Number 21); and a buffer, having at least one trigger (See Column 2 Lines 23-26), integrated on a component coupled with a bus (See Figure 1 and Column 2 Lines 23-26), to facilitate observing and echoing a plurality of signals transmitted on a bus (See Figure 1 and Column 2 Lines 23-26), wherein the trigger operates to instruct the buffer using a control signal-based indication (See Column 2 Lines 23-31). Tanaka teaches the use of a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and

Column 1 Lines 9-55). Gonzales does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Gonzales with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 14, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

26. Claims 1, 6, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,903,719 to Yamamoto ("Yamamoto"), Tanaka, and knowledge commonly known in the art.

27. In reference to Claim 1, Yamamoto teaches a buffer having a trigger (See Figure 2 Number 18 and Column 2 Lines 23-26), integrated on a component connected with a bus (See Figure 2 and Column 2 Lines 3-5), to facilitate observing and echoing a plurality of signals transmitted on said bus (See Column 2 Lines 35-44), wherein the trigger operates to instruct the buffer using a control signal-based indication (See Column 2 Lines 35-38). Yamamoto does not teach that the bus is a

simultaneous bi-directional (SBD) memory bus having ternary logic levels. Tanaka teaches the use of a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55). The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Yamamoto with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 1, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

28. In reference to Claim 6, Yamamoto teaches a buffer having a trigger (See Figure 2 Number 18 and Column 2 Lines 23-26), integrated on a component connected with a bus (See Figure 2 and Column 2 Lines 3-5), to facilitate observing and echoing a plurality of signals transmitted on the bus (See Column 2 Lines 35-44), wherein the trigger operates to instruct the buffer using a control signal-based indication (See Column 2 Lines 35-38). Yamamoto does not transmitting signals on a simultaneous bi-directional (SBD) memory bus having ternary logic levels. Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55). The Examiner takes Official Notice that a

memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Yamamoto with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 6, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

29. In reference to Claim 14, Yamamoto teaches a memory (See Figure 2 Number 12); an I/O port (See Figure 2 Number 17); a microprocessor (See Figure 2 Number 11); and a buffer, having a trigger (See Figure 2 Number 18 and Column 2 Lines 23-26), integrated on a component coupled with a bus (See Figure 2 and Column 2 Lines 3-5), to facilitate observing and echoing a plurality of signals transmitted on a bus (See Column 2 Lines 35-44), wherein the trigger operates to instruct the buffer using a control signal-based indication (See Column 2 Lines 35-38). Yamamoto does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55). The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in

the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Yamamoto with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 14, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

30. Claims 1, 6, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,119,254 to Assouad et al. ("Assouad"), Tanaka, and knowledge commonly known in the art.

31. In reference to Claim 1, Assouad teaches a buffer having a trigger (See Column 7 Lines 43-46), integrated on a component connected with a bus (See Figure 3 Numbers 104 and 105), to facilitate observing and echoing a plurality of signals transmitted on said bus (See Column 7 Lines 50-62), wherein the trigger operates to instruct the buffer using a control signal-based indication (See Column 7 Lines 43-46). Assouad does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55). The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown

to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Assouad with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 1, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

32. In reference to Claim 6, Assouad teaches a buffer having a trigger (See Column 7 Lines 43-46), integrated on a component connected with a bus (See Figure 3 Numbers 104 and 105), to facilitate observing and echoing a plurality of signals transmitted on the bus (See Column 7 Lines 50-62), wherein the trigger operates to instruct the buffer using a control signal-based indication (See Column 7 Lines 43-46). Assouad does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55). The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Assouad with the simultaneous bi-

directional bus of Tanaka, resulting in the invention of Claim 6, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

33. In reference to Claim 14, Assouad teaches a memory (See Figure 3 Number 112); an I/O port (See Figure 3 Number 204); a microprocessor (See Figure 3 Number 111); and a buffer, having a trigger (See Column 7 Lines 43-46), integrated on a component coupled to a bus (See Figure 3 Numbers 104 and 105), to facilitate observing and echoing a plurality of signals transmitted on a bus (See Column 7 Lines 50-62), wherein the trigger operates to instruct the buffer using a control signal-based indication (See Column 7 Lines 43-46). Assouad does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55). The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Assouad with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 16, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

Response to Arguments

34. Applicant's arguments filed 3 February 2005 have been fully considered but they are not persuasive.

35. Applicant has argued that Dabral does not disclose or reasonably suggest a buffer having a trigger to instruct the buffer using one or more of a control signal-based indication, and address signal-based indication, and a time-based indication. In response, the Examiner notes that, as shown in the above rejections, Dabral discloses that the trigger operates to instruct the buffer using a control signal based indication (See Column 1 Lines 14-17 and Column 3 Lines 7-10), and a time-based indication (See Column 1 Lines 14-17). The trigger of Dabral will inherently instruct the buffer using an address-signal based indication, as the device of Dabral is used in a system for transferring data between devices that include processors, storage devices, and I/O devices (See Column 1 Lines 12-14), and as such would inherently include address signals.

36. Applicant has argued that La Joie, Tanaka, Gonzales, Yamamoto, and Assouad, neither individually nor when combined in any combination, disclose or reasonably suggest a buffer having a trigger to instruct the buffer using one or more of a control signal-based indication, and address signal-based indication, and a time-

based indication. In response, the Examiner notes that, as shown in the above rejections, La Joie teaches that the trigger operates to instruct the buffer using a control signal-based indication (See Column 13 Lines 36-42 of La Joie); Tanaka is not being relied upon to teach this limitation; Gonzales teaches that the trigger operates to instruct the buffer using a control signal-based indication (See Column 2 Lines 23-31 of Gonzales); Yamamoto teaches that the trigger operates to instruct the buffer using a control signal-based indication (See Column 2 Lines 35-38 of Yamamoto); and Assouad teaches that the trigger operates to instruct the buffer using a control signal-based indication (See Column 7 Lines 43-46 of Assouad).

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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TJC

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